We claim:

1. A semiconductor configuration, comprising:

a semiconductor body including a first connection zone of a first conductivity type, a second connection zone of the first conductivity type, a channel zone of the first conductivity type, at least one control electrode, and an insulation layer;

said channel zone of the first conductivity type being formed between said first connection zone and said second connection zone;

said insulation layer surrounding said at least one control electrode;

said at least one control electrode extending, adjacent to said channel zone, from said first connection zone to said second connection zone;

said semiconductor body defining a vertical direction and a lateral direction; and

said first connection zone, said second connection zone and said at least one control electrode extending in the vertical direction such that, when a voltage is applied between said

first and second connection zones, a current path along the lateral direction is formed in the channel zone.

2. The semiconductor configuration according to claim 1, wherein:

said first connection zone and said second connection zone define the lateral direction as extending from said first connection zone to said second connection zone;

at least one of said first and second connection zones has a first dimension in the vertical direction and a second dimension in the lateral direction; and

said first dimension is smaller than said second dimension.

3. The semiconductor configuration according to claim 1, wherein:

the lateral direction is a first lateral direction extending from said first connection zone to said second connection zone;

said semiconductor body defines a second lateral direction transverse to the first lateral direction;

said at least one control electrode is a substantially plate-shaped control electrode having a respective longitudinal extent in the vertical direction and in the first lateral direction and a lateral extent in the second lateral direction; and

said respective longitudinal extent is greater than said lateral extent.

4. The semiconductor configuration according to claim 1, wherein:

said first connection zone has a first zone with a first dopant concentration and a second zone with a second dopant concentration;

said first dopant concentration is higher than said second dopant concentration; and

said second zone is formed between said first zone and said channel zone.

5. The semiconductor configuration according to claim 1, wherein:

said first connection zone has a first zone with a first dopant concentration and a second zone with a second dopant concentration; and

said second zone completely surrounds said first zone in the lateral direction.

6. The semiconductor configuration according to claim 1, wherein:

said first connection zone has a first zone with a first dopant concentration and a second zone with a second dopant concentration;

said second connection zone has a third dopant concentration;

said channel zone has a fourth dopant concentration; and

said fourth dopant concentration is lower than said first and third dopant concentrations.

7. The semiconductor configuration according to claim 1, wherein:

said semiconductor body has a rear side;

a layer of the first conductivity type is disposed at said rear side;

said first connection zone has a first zone with a first dopant concentration and a second zone with a second dopant concentration;

said layer has a third dopant concentration;

said third dopant concentration substantially corresponds to said first dopant concentration; and

said layer is connected to said first connection zone.

8. The semiconductor configuration according to claim 1, including:

a further first connection zone;

a further channel zone extending between said further first connection zone and said second connection zone; and

said at least one control electrode extending, adjacent to said second connection zone, said channel zone and said further channel zone, from said first connection zone to said further first connection zone.

9. The semiconductor configuration according to claim 1, wherein:

said semiconductor body has a front side and a rear side; and

said first connection zone extends, in the vertical direction, from said front side to said rear side of said semiconductor body.

10. The semiconductor configuration according to claim 1, wherein:

said semiconductor body has a rear side; and

an electrically conductive layer is disposed on said rear side of said semiconductor body for making contact with said first connection zone.

11. The semiconductor configuration according to claim 1, including an electrically conductive zone introduced in said first connection zone for making contact with said first connection zone.

12. The semiconductor configuration according to claim ~~11~~, wherein said electrically conductive zone is formed of a

material selected from the group consisting of polysilicon and a metal.

13. The semiconductor configuration according to claim 1, including:

an electrically conductive zone introduced in said second connection zone for making contact with said second connection zone.

14. The semiconductor configuration according to claim 13, wherein said electrically conductive zone is formed of a material selected from the group consisting of polysilicon and a metal.

15. The semiconductor configuration according to claim 1, wherein said first dopant concentration is higher than 10^{18} cm^{-3}.

16. The semiconductor configuration according to claim 1, wherein said second dopant concentration is substantially 5×10^{15} cm^{-3}.

17. The semiconductor configuration according to claim 6, wherein said fourth dopant concentration is less than 10^{14} cm^{-3}.